REMARKS

This paper is responsive to the Non-Final Office Action dated October 13, 2004. Claims 1-56 were examined.

Claim Rejections - 35 U.S.C. § 112

Claims 25 and 27 stand as rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully traverses this rejection.

Regarding claim 25, the Examiner has questioned the limitation "wherein X-lines comprise bit lines." Such claim, along with claim 24, is presented to reinforce that the invention, while described in the context of many exemplary embodiments using a common terminology of X-lines being also known as word lines, is readable on structures irrespective of whether such X-lines, as claimed, are viewed as word lines or bit lines in terms of memory array organization.

Regarding claim 27, the Examiner has questioned how the claimed limitations relate to claim 1. Claim 27 adds the limitation that each of the first Y-line group is configured to be logically identical in a read mode of operation, and each of the second Y-line group is configured to be logically identical in a read mode of operation. Examples of a structure illustrating this limitation include that shown in Fig. 6 (the first Y-line group including BL1-BL4 and the second Y-line group including BL5-BL8), and also that shown in Fig. 7, Fig. 8, Fig. 9, and Fig. 11.

Claim Rejections - 35 U.S.C. § 103

Claims 1-5, 8, 9, 13-24, 26, 28-33, 37-43, 46-53 and 56 stand as rejected under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi, et al. (U. S. Patent No. 5,337,281) in view of Kato, et al. (U. S. Patent No. 6,741,509). Applicant respectfully traverses this rejection.

Regarding claim 1, the Examiner has admitted that Kobayashi fails to disclose X-lines configured to be logically identical in a read mode of operation, and has relied upon Kato for allegedly providing this teaching, citing primarily three passages (column 43, lines 37-49; column 47, lines 55-65; column 61, lines 35-39). Applicant respectfully submits that Kato nowhere teaches X-lines configured to be *logically identical* in a *read* mode of operation.

Kato discloses a memory array in which more than one word line may be simultaneously activated, but such word lines may be located within different memory blocks. The number of word lines which can be used to simultaneously read/write independent data items in the memory cell array is determined by the data line configuration in the memory cell array. For example, in certain embodiments, a total of 16 Master DQ line pairs (MDQP) are used to access data within the memory cell array, which are each coupled to a respective one-fourth of the memory array (i.e., in Fig. 59, MDQPa<0:3> coupled to sense amplifier banks within region "a", MDQPb<0:3> coupled to sense amplifier banks within region "b", etc.) (See column 43, line 50 through column 44, line 21) The total number of word lines used to simultaneously read/write independent data is thus four.

Such simultaneously activated word lines are *not* logically identical, since each corresponds to a unique row address. Moreover, each of these word lines is associated with a different block, and thus different bit line groups, and each corresponds to unique data read from the array.

Kato also discloses certain embodiments including sequentially accessing more than one word line, in which once-activated word lines are held in the activated state during a plurality of successive word line selection cycles. For example, in Figs. 5-12 Kato discloses a memory cell array having a stacked-word-line test mode (i.e., a "Multiple WL test Mode") in which more than one word line is simultaneously activated, and in which

> the number of word lines which can be activated for some bit line pairs and sense amplifiers associated therewith (which are collective referred to as a memory block) is only one. Further, when the sense amplifiers are commonly used or shared by adjacent memory blocks (shared sense amplifier), the word line can be selected in only either of the memory blocks which commonly use the sense amplifiers. In other words, a maximum of N/2 word lines can be selected in a memory cell array having N memory blocks. (Column 11, lines 44-56)

None of the simultaneously selected word lines are associated with the same bit line group. Moreover, such word lines are also sequentially selected, and each corresponds to a unique row address. In many other embodiments, the number of simultaneously selected word lines is also at most one per memory block.

Kato also discloses certain embodiments including a stacked-word-line *test mode* in which more than one word line is simultaneously activated within the *same* memory block. However, such embodiments are subject to the limitation that the contents of memory cells connected to a plurality of word lines selected in the memory block must be the same on the identical column. Otherwise data destruction will occur. (Column 27, lines 54-65) Such word lines are driven *sequentially* (column 31, lines 10-11), each responsive to a unique row address, and thus cannot be considered to be configured logically identical.

As described, the first word line in the block is activated and the sense amplifiers activated to sense and latch data on the bit lines. Then , in the second cycle, the sense amplifier is already activated before the second word line is driven active. The sense operation of the bit line is terminated and the state is held. The same data as those of the memory cells connected to the first selected word line are *written* into second selected word line in the same memory block when the second word line is selected and the word line potential rises. (column 31, line 62 through column 32, line 5) The second word line to be selected in a memory block cannot be read, but only written with the data previously read from the first selected word line. Such *sequential, non-read* mode of operation cannot be viewed as being two word lines configured to be logically identical in a read mode of operation.

In the first passage cited by the Examiner (column 43, lines 36-49), the embodiment described specifically requires that the four simultaneously activated word lines cannot be activated in the identical memory block nor in adjacent memory blocks (if using shared sense amplifiers) in order to prevent occurrence of data destruction (lines 44-49). Each of these word lines is associated with a unique row address. Moreover, each is associated with a different memory block, and thus different bit line groups.

In the second passage cited by the Examiner (column 47, lines 55-65), the embodiment described specifically states that independent data items can be simultaneously read/written with respect to four total word lines, one selected from each of regions "a", "b", "c", and "d" in Fig. 59 (lines 60-62). Each of these word lines is associated with a unique row address. Moreover, each is associated with a different memory block, and thus different bit line groups.

In the third passage cited by the Examiner (column 61, lines 35-39), the cited text describes

> word lines which are activated together in the memory cell array and used for reading/writing independent data simultaneously based on the data line configuration are set to read/write independent data items are set to belong to the same repair region. [sic]

Such a structure is described above, and refers to the data line structures (e.g., the MDQP lines) and their organization with respect to the memory cell array. Such simultaneously activated word lines are not within the same memory block, as described above. Each of these word lines is associated with a unique row address. Moreover, each is associated with a different memory block, and thus different bit line groups.

While not specifically cited by the Examiner, Kato continues the description of the embodiment (column 61 at lines 42-47) as stating that

> the number of word lines which can be connected to the same bit line via cell transistors and activated together in the same repair region in an operation mode which holds once activated word lines in the activated state in a plurality of successive word line selection cycles (for example, in a stacked-word-line test mode) is set to a maximum.

Such operation, as is previously described above, cannot be viewed as being more than one word line configured to be logically identical in a read mode of operation, as alleged by the Examiner.

Regarding the other independent claims 29, 38 and 51, and all the dependent claims, the Examiner has offered no references or other support for the rejection. Applicant respectfully traverses the rejection of claims 2-56 and believes that no *prima facie* case for the rejection has been established.

Claims 1-5, 8-24, 26, 28-56 stand as rejected under 35 U.S.C. § 103(a) as being unpatentable over Scheuerlein, et al. (U. S. Publication No. 2004-0100852) in view of Kato, et al. (U. S. Patent No. 6,741,509). Applicant respectfully traverses this rejection.

Regarding claim 1, the Examiner has admitted that Scheuerlein fails to disclose X-lines configured to be logically identical in a read mode of operation, and has again relied upon Kato for allegedly providing this teaching, citing the same three passages. The Examiner has presented the same argument, with the same conclusion.

Applicant again traverses the rejection for the same reasons as explained above. Specifically, the rejection of claim 1 is traversed for the many reasons enumerated above, and the rejection of claims 2-56 is traversed for lack of a *prima facie* case having been established for the rejection. Applicant notes, however, that after listing precisely the same argument and alleged disclosure of Scheuerlein and Kato compared to Kobayashi and Kato, the Examiner arrives at a second different group of rejected claims without any explanation, comment, or support. Such observation underscores Applicants contention that a *prima facie* case has not been made on the record for the benefit of aiding Applicant's ability to respond.

Claims 1-10, 12, 14-24, 26, 28-34, 36, 38-44 and 47-54 stand as rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwata, et al. (U. S. Publication No. 2003-0161197) in view of Kato, et al. (U. S. Patent No. 6,741,509). Applicant respectfully traverses this rejection.

Regarding claim 1, the Examiner has admitted that Iwata fails to disclose X-lines configured to be logically identical in a read mode of operation, and has again relied upon Kato for allegedly providing this teaching, citing the same three passages.

Applicant again traverses the rejection for the same reasons as explained above. Specifically, the rejection of claim 1 is traversed for the many reasons enumerated above.

The Examiner has offered a reference in support of the rejection of dependent claims 3-7 and 41, citing Iwata. Such claims are believed allowable at least for their dependence from an allowable independent claim. The rejection of the remaining claims 2, 8-10, 12, 14-24, 26, 28-34, 36, 38-40, 42-44 and 47-54 is traversed for lack of a *prima facie* case having been established for the rejection. Applicant again notes that after listing precisely the same argument and alleged disclosure of Iwata and Kato compared to Scheuerlein and Kato (and compared to Kobayashi and Kato), the Examiner arrives at a third different group of rejected claims. Such observation

underscores Applicants contention that a *prima facie* case has not been made on the record for the benefit of aiding Applicant's ability to respond.

Looking back at these three grounds of rejection, Applicant submits that, at best, the cited references (particularly Kato) disclose activating during a read mode a single word line in each of several memory array blocks, and in a certain test mode, activating more than one word line in a memory array block. Such a test mode is described as useful for voltage stressing a memory array (e.g., Kato, at column 53, lines 1-7), cannot be used in a read mode if more than one word line per memory block is activated, and when used the identical data must be previously written into memory cells associated with each word line.

There is nothing in the teaching of Kato, combined with either of Kobayashi, Scheuerlein, or Iwata to suggest a non-volatile memory cell array comprising a first plurality of X-lines configured to be logically identical in a read mode of operation, and each associated with a first Y-line group numbering at least one Y-line, as recited in Applicant's claim 1. Even assuming, *arguendo*, that these references are so combined, the teaching of these four references still does not arrive at the claimed limitation. Consequently, Applicant respectfully requests the rejections be withdrawn.

Summary

Claims 1-56 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited.

Should any issues remain, Applicant respectfully requests a telephonic interview with the Examiner to discuss this response, and further in the hope that the remaining issues might be efficiently resolved.

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Andrew C. Graham — 1-13-05 Date

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